ABSTRACT OF THE DISCLOSURE

[0039] Presented herein are systems and methods for two address map for transactions between an X-bit processor and a Y-bit wide memory. A processor subsystem comprises a first address space, a second address space, and a bridge. The first address space stores data words of a first length. The second address space stores data words of a second length. The bridge performs one transaction after receiving a transaction with an address corresponding to the first address space and performs two transactions after receiving a transaction with the address corresponding to the second address space.